

EAST - [default.wsp:1]

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☐ Drafts
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☒ **Active**
☐ L2: (1) memory with (latch near3 circuit) with (in:
☐ L3: (1) memory with (latch near3 circuit) with (in:
☐ L4: (1) memory with (latch near3 circuit) with (in:
☐ L5: (122) memory with (latch near3 circuit) and (:
☐ L6: (5) memory with (latch near3 circuit) with (in:
☐ Failed
☐ Saved

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 DBs US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
 Default operator: OR
☒ Plural
☒ Highlight all hit terms initially

BRS form IS&R form Image Text HTML

	Type	L #	Hits	Search Text	DBs
1	BRS	L2	1	memory with (latch near3 circuit) with (insulat\$3 near3 gate) with (back near3 gate) with substrate with (potential or bias or volt\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L3	1	memory with (latch near3 circuit) with (insulat\$3 near3 gate) with (back near3 gate) with substrate and (potential or bias or volt\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L4	1	memory with (latch near3 circuit) with (insulat\$3 near3 gate) with (back near3 gate) and substrate and (potential or bias or volt\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L5	122	memory with (latch near3 circuit) and (insulat\$3 near3 gate) and (back near3 gate) and substrate and (potential or bias or volt\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
5	BRS	L6	5	memory with (latch near3 circuit) with (insulat\$3 near3 gate) and (back near3 gate) and substrate and (potential or bias or volt\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB

☒ Hits
☐ Details
☒ HTML

Ready

NUM

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DBs US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB

Default operator: OR

Plurals

Highlight all hit terms initially

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Active

- L14: (1) memory with cross-coupled with (substrate adj (potential or bias or volt\$3))
- L16: (0) 15 with (back adj gate)
- L15: (50) memory with sram with (substrate adj (potential or bias or volt\$3))
- L17: (2) 15 same (back adj gate)
- L18: (13) 15 and (back adj gate)
- L19: (0) 15 with ((back adj gate) or back-gate)
- L20: (2) 15 same ((back adj gate) or back-gate)
- L21: (13) 15 and ((back adj gate) or back-gate)

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BRS form IS&R form Image Text HTML

	Type	L #	Hits	Search Text	DBs
1	BRS	L14	1	memory with cross-coupled with (substrate adj (potential or bias or volt\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L16	0	15 with (back adj gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L15	50	memory with sram with (substrate adj (potential or bias or volt\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L17	2	15 same (back adj gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
5	BRS	L18	13	15 and (back adj gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L19	0	15 with ((back adj gate) or back-gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L20	2	15 same ((back adj gate) or back-gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L21	13	15 and ((back adj gate) or back-gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB

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